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# Current Mode Monolithic Active Pixel Sensor With Correlated Double Sampling for Charged Particle Detection

Michal A. Szelezniak, Grzegorz W. Deptuch, *Member, IEEE*, Fabrice Guilloux, Sébastien Heini, and Abdelkader Himmi

**Abstract**—A monolithic active pixel sensor operating in current mode for charged particle detection is described. The sensing element in each pixel is an n-well/p-sub diode with a PMOS transistor integrated in an n-well. The drop of the n-well potential from the collection of charge modulates the transistor channel current. Each pixel features two current mode memory cells. The subtraction of distant-in-time samples frees the signal of fixed pattern noise (FPN) and of the correlated low-frequency temporal noise components, resulting in extraction of the particle footprint. The subtraction circuits are placed at each column end. A transimpedance amplifier, integrating in sequence two current samples and subtracting the results in an arithmetic operation, was adopted. The integrated version of the transimpedance amplifier, designed with a maximized conversion gain, is burdened by a risk of an early saturation, imperiling its operation, if the dispersions of the dc current component are too big. The degree of dispersions could not be estimated during the design. Some number of columns is available as a backup with the direct current readout. An external realization of the subtracting circuit, based on the same principle, is used to process direct output columns. The concept of the data acquisition setup developed, the tested performance of an array of cells, and the processing circuitry are described.

**Index Terms**—Active pixel sensors, correlated double sampling, current integrating transimpedance amplifier, current mode imager, parallel column readout, particle detector.

## I. INTRODUCTION

**I**NCREASING requirements for particle tracking in future particle physics experiments, especially leading to the unprecedented designs of vertex detectors, and challenges in nuclear imaging in medicine, material science, and biology raise new demands for silicon sensors. Emerging in the last decade, monolithic active pixel sensors (MAPSs) became quickly credible competitors to charge-coupled devices and hybrid pixel sensors (HPSs), which are widely used nowadays in these fields (see, for example, [1] and [2]). It is hardly possible that MAPS

will not supersede these technologies. Although lacking the advantages of HPSs, like radiation hardness, timing resolution, thick active volume of the detector, and the power of advanced parallel signal processing in each pixel, MAPSs may be superior over a wide spectrum of specific applications since they offer a thin device that does not disrupt traversing particles and that combines high spatial resolution, design flexibility, and cost efficiency. The key point is the integration of the detector and the processing part on a single integrated circuit using a standard CMOS process. The core of the device is an array of pixels, containing a sensing element and components of the first stage of the readout chain. As is the usual approach, the sensing element is a diode of the n-well/p-epi, or more general n-well/p-sub, type that generates voltage signals proportional to the amount of the charge liberated by an impinging particle. The most standard pixel design is the three transistor (3T) architecture, known from visible light cameras [3].

Applications in high-energy physics require large area and high granularity sensors. The resolving capabilities of the whole detector complex for individual physical events translate to requirements for fast readout of data from detector subunits, such as layers, barrels, etc., constituting the whole system [4]. The readout requirement implies higher than usual data throughputs. The solution, reducing the data throughput in the transfer to the acquisition system, is a sparsification done on the chip. The ultimate goal for the on-chip processing is signal discrimination and encoding of positions of impinging particles.

The usual sensor operation consists of conversion of the collected charge to voltage inside a pixel and further processing of voltage signals [5]. Detectors with pixels, generating current signals, are an alternative to the voltage mode pixels. Two examples of such pixels may be DEPFET, realized on a high resistivity silicon substrate [6], and PMOSFET, with gate and n-well tied together and left floating, realized in a silicon-on-insulator process [7]. A new scheme for the operation in a current mode, called PhotoFET, was proposed, bearing realization in a standard CMOS process [8]. The advantages of a current mode operation are high swings of the output signals regardless of power supply voltages and an ease of implementation of a basic signal treatment with arithmetic operations, such as addition and subtraction [9], on a pixel and a chip level.

The first results, obtained by the LEPSI/IReS group with a simple, single pixel PhotoFET test structure, were encouraging. The tests with a  $^{55}\text{Fe}$  source and a pixel signal sampled in an interval of about 1 ms showed sensitivity of about  $330 \text{ pA/e}^-$ ,

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at a constant dc bias current of about 5  $\mu\text{A}$ . The direct current output of the PhotoFET cell was connected for the continuous conversion to a discrete, resistive feedback transimpedance amplifier. The lack of any switching activity, high conversion gain, and narrow frequency bandwidth (over a dozen megahertz) of the setup allowed the achievement of good noise performance. The design of the minimum ionizing MOS active pixel sensor (MIMOSA) VII (MVII) aimed to validate the adequacy of an array of PhotoFET cells as a high sensitivity device in tracking of charged particles.

The charge collecting diode in the PhotoFET cell works in the so-called continuous reverse biasing scheme (CRB) with a forward biased diode connected to the power supply voltage. This mode of operation is different from the standard diode in a 3T pixel structure. For CRB, the extraction of signals from particles, impinging at different times, requires the subtraction of two distant-in-time samples. This operation is equivalent to correlated double sampling (CDS) processing. This term is used in this paper for describing the process of subtracting two samples, aimed at the extraction of signals generated by impinging particles.

The first part of this paper describes the architecture of the sensor, built as an array of pixels based on the PhotoFET sensing element. The second part presents the flexible data acquisition system developed for testing the sensor. The following sections, dedicated to the measurement results, describe operation of the PhotoFET cells and present a crosscheck between the results obtained in software offline data processing and the results from the hardware realization of the CDS operation. A scheme for realization of the integrated CDS and some measurement results for this circuit are also presented. In the conclusion section, pros and cons of the discussed structure are reviewed and possibilities of the on-chip data sparsification are weighed.

## II. TESTING ENVIRONMENT

### A. Architecture of the Sensor

1) *Chip Structure*: The test sensor MVII was implemented in a commercial 0.35  $\mu\text{m}$  process to validate prior single pixel performance in a matrix array, including parasitic effects. The latter include process variation, switching effects, bias shifts from coupling of digital signals, charge injection, etc. A synoptical diagram of the MVII chip is sketched in Fig. 1. The device contains an array of  $18 \times 64$  pixels with two dummy boundary columns not connected to the readout circuitry. All 16 columns have their own buffering blocks for parallel readout. The digital sequencer, programmable from outside with a custom serial port interface, controls the operation of the chip. It consists of a set of circular shift registers, propagating a loaded pattern (left side of Fig. 1). One part of the sequencer asserts a series of signals needed to perform sampling operations in the pixel and select individual cells for readout. The second part of the sequencer orchestrates the column level readout circuitry synchronously with access to rows of pixels. In the case of a discrete realization of the readout circuitry, presented later in this paper, the synchronization was achieved by reproducing the required logic signals from the MVII core in the Complex Programmable Logic Device (CPLD) chip. One complete readout of the chip, starting

at the first row and finishing at the last one, is referred to as a frame. The sensor is read out in a continuous way without any dead time between frames.

The first eight columns of the array are processed by the block of eight current integrating transimpedance amplifiers, described in one of the next sections. The current signals from pixels are converted to voltages and subtracted. The resulting signals are read out on eight dedicated pads. This readout chain embodies a novel realization of the on-chip CDS processing. Current integrating transimpedance amplifiers are very sensitive to the dc component of the integrated current signal. The design of the amplifiers was driven by maximization of the gain, assuming that the average value of the current for all pixels can be subtracted at the input of the amplifier. The signal swing should allow some room for pixel-to-pixel dispersions of the dc component. Dispersions that are too large may endanger the transimpedance amplifiers, leading to their saturation. The degree of dispersion could not be estimated during the design. Thus, the second eight columns were designed as a backup with the direct current readout. These columns are not subjected to any processing on the chip, giving a direct access to the current signals. The current from these pixels can be read out directly or after amplification by a factor of ten with a block of eight current amplifiers, as is shown in the bottom part of Fig. 1.

The operation of the chip requires only one clock signal with a frequency of up to 100 MHz. This clock shifts the sequence controlling the transimpedance amplifiers. The pattern, sent to rows, is propagated with clocks derived from the main clock with division by ten and six, reducing the switching activity in the chip.

2) *Pixel Architecture*: The CRB bias scheme, present in the PhotoFET cell, is specifically adapted to low illumination levels and low individual signal amplitudes. These conditions are met in a typical vertex detector (e.g., see note on STAR upgrade requirements [10]). The CRB scheme has a natural feature of signal accumulation from different events on the capacitance of the charge collecting diode if the time between these events is shorter than the time of the recharge. Hence, the extraction of signals due to particles is impossible by a simple subtraction of a constant reference value from the actual sample. The data processing algorithm, allowing subtraction of two samples separated in time, is required. The integration of two memory cells within each pixel is required to achieve this goal. If the sampling is done periodically, e.g., with a cadence of the full frame readout, the correlated components of the signal vanish in the result of the subtraction, improving the noise performance.

The architecture of the pixel, containing two memory cells, is presented in Fig. 2. The PhotoFET charge-sensing element is built of the n-well/p-epi charge collecting diode and transistors  $M1$  (PMOS) and  $M2$  (NMOS). The collected charge alters the threshold voltage of  $M1$  through the drop of the n-well potential and hence modulates the channel current of the transistor  $M1$ . The sensitivity is increased by applying the n-well potential to the gate of  $M1$  via the source follower transistor  $M2$  [11]. The source region of the transistor  $M1$  is an anode of the forward biased diode in the CRB scheme. The PhotoFET current consists of a dc component (on the order of several microamperes) and a signal originating from an impinging particle (on

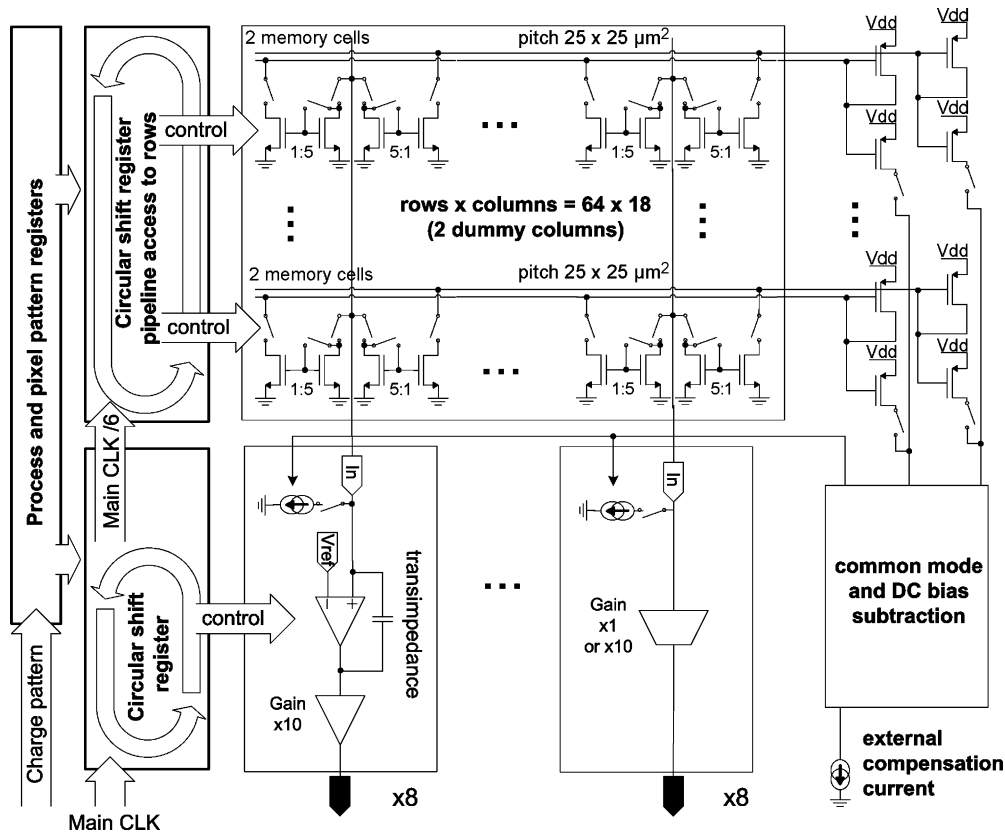


Fig. 1. Block diagram of the MIMOSA VII chip.

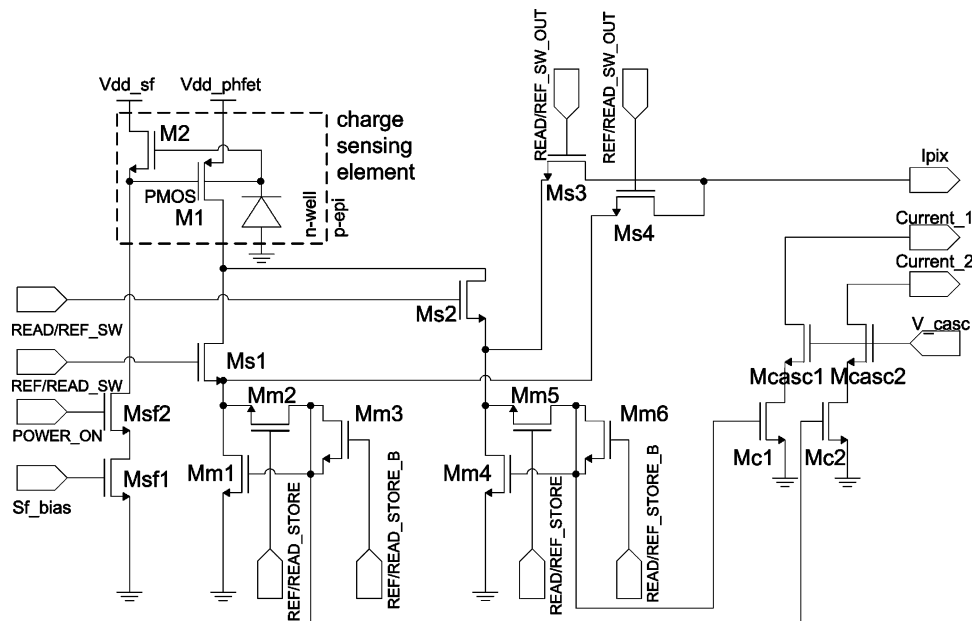


Fig. 2. Schematic diagram of the pixel from the MIMOSA VII chip.

the order of nanoamperes). The dc component, not conveying any useful information, has to be subtracted to avoid saturation of the transimpedance amplifiers at the column ends. An attempt to subtract a reference current inside each pixel was made in the past in [12] but resulted in poor accuracy, as the sampled current had a significant offset compared to the reference. The on-chip circuitry in MVII allows the subtraction of the dc current com-

ponent defined by an external source or a mean value calculated on the chip. The second option yielded higher noise and was not exploited in the tests.

A charge sensing element operating in current mode encourages the use of current memory cells in each pixel. The number of memory cells is arbitrarily limited by the constraints on the pixel size. Two memory cells are sufficient for extraction of sig-

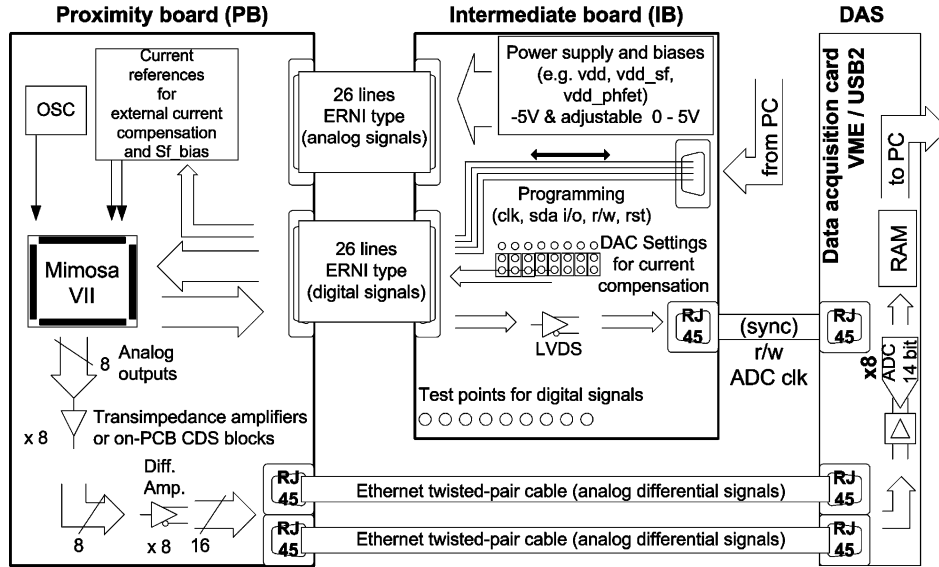


Fig. 3. Simplified view of the test system.

nals generated by particles by subtracting two consecutive samples. The presented design features two current mode memory cells, built with transistors  $Mm1 - 3$  ( $Mem1$ ) and  $Mm4 - 6$  ( $Mem2$ ), as shown in Fig. 2. The gate-to-source capacitances of the transistors  $Mm1$  and  $Mm4$  store voltages corresponding to the sampled currents.

The access to an individual pixel is divided into two phases, i.e., the write phase and the read phase. In the first phase, an actual current value is sampled on one of the memory cells. The second memory cell always stores a sample from the previous access. During the second phase, both current samples are sent sequentially on the  $I_{pix}$  terminal for readout by activating the switches  $Ms3$  and  $Ms4$  in the proper order. The access to rows is pipelined, i.e., two consecutive rows of pixels are processed simultaneously. When the leading row is being read out, current sampling is performed in the following row.

Taking signal samples into the memory cells is accomplished in turns. For the sake of distinction, the notion of even and odd frames can be introduced. Every even frame goes to  $Mem1$  and every odd frame goes to  $Mem2$ . During the readout phase, both current samples are read out successively. The reading order of the stored samples is alternated every frame. In the case of an even frame, the contents of  $Mem1$  are, followed by the contents of  $Mem2$ . For odd frames, the order is reversed. This allows the column-end circuitry to subtract the reference level from the actual one resulting in one desirable polarity of the electrical signal as a response to the particle impact. The readout is column parallel.

The matrix of pixels is divided horizontally into three sub-blocks. Each row contains pixels of the same type. The first 32 rows are built of pixels with 100 fF capacitances in the memory cells and with charge injection compensation switches. The switches are shown in Fig. 2 as transistors  $Mm3$  and  $Mm6$ . The next 16 rows contain pixels with the same capacitance value but with the compensating switches unconnected to the driving lines. Pixels in the last 16 rows contain 50 fF storing capacitors with active switches for charge injection compensa-

tion. The pixel size is  $25 \times 25 \mu m^2$ . Transistors  $Mc1$  and  $Mc2$  belong to the system for deriving the mean current for each row.

### B. Test Bench

1) *Test Environment:* Different readout schemes allowed the extraction of different information about the chip. First, the functionality of the PhotoFET cells in an array structure was tested using direct current outputs with off-chip transimpedance amplifiers and software analysis of the recorded raw data. When dc current components showed significant pixel-to-pixel dispersions, an external subtracting circuit, based on the same principle as the integrated on-chip amplifier, was used to process current signals. Lastly, accessible tests were performed using the high gain in-chip CDS amplifier.

The schematic diagram, shown in Fig. 3, presents a general view of the setup. The test system consisted of three main parts: the proximity board (PB) on which the chip under test was seated, the intermediate board (IB), and the acquisition card, being the main part of the data acquisition system (DAS). The modular structure of the system was mandatory for intended tests of the detector with minimum ionizing particles. The testing environment included a modest and closed volume with controlled temperature for the card hosting the chip, imposing limitations on the PB size and restrictions on power dissipation. The acquisition system was located a remote distance from the device under testing, requiring long connection cables. The chip and DAS were in a master-slave configuration with the clock signal, sequencing operation of the chip, generated locally on the PB. The MVII provided a flag showing validity of the analog data for synchronizing data acquisition. The flag signal was used in DAS directly as its analog-to-digital conversion clock. Another component of the system was a small auxiliary card with the bare MVII die bonded. The card contained decoupling capacitors and miniaturized multipin connectors for plugging it onto PB and allowing chip replacements.

2) *Proximity Cards:* Two versions of the PB were designed to separate testing of the direct current outputs and the on-chip

CDS from the integrated CDS implementation. The PB circuitry processed the MVII signals and converted them into a differential mode for interfacing with the DAS. The cards hosted two current sources. The reference for the PhotoFET source follower (transistors  $M2$  and  $Msf1$  in Fig. 2) was tunable from a few tens of nanoamperes up to a few microamperes with a load resistance. A dc current value, subtracted from the PhotoFET current, was tunable from a few tens of nanoamperes to about 50  $\mu\text{A}$  with a local DAC and an 8-bit word defined on the IB. One of the cards transferred, according to its configuration, direct current signals or CDS processed voltages to the remote DAS by, correspondingly, resistive feedback transimpedance amplifiers (about 13 k $\Omega$  transresistance) or operational amplifier buffers, both coupled to differential drivers with the gain of about 1.5 (eight channels). The whole readout chain was designed to be fast, low-noise, and to operate at the main clock frequency of up to 100 MHz.<sup>1</sup> The second card equipped with integrated circuits for CDS operation, presented in detail in the following sections, hosted a programmable logic device for providing a correct sequence for activating switches in the CDS blocks (in four channels) in pace with the operation of the MVII chip.

3) *Intermediate Board*: The IB hosted reference voltage regulators, buffers, and low-voltage differential signal converters for digital signals sent to the DAS and the interface between the chip and the PC.

4) *Data Acquisition System*: The DAS was based on analog-to-digital conversion boards connected to a PC for storing the data. Each board was equipped with four differential analog channels connected to fast 12-bit ADCs achieving a least significant bit resolution equal to 500  $\mu\text{V}$  [13]. Depending on the readout scheme and the number of channels to be acquired, one or two cards were used. Signals incoming to DAS were buffered and distributed onto two lines, assuring synchronous operation of the two cards. Accessing direct current outputs required registering two samples per single pixel readout, corresponding to two memory cells, as opposed to CDS processed outputs with one sample per pixel to store.

### III. PHOTOFET MEASUREMENT RESULTS

#### A. Acquisition of Direct Current Outputs and Software Analysis

1) *Pixel Characterization*: The tests performed on direct currents outputs allowed an insight into the operation of individual PhotoFET cells. The tests started with the reference settings matching prior simulations and measurements performed on a single cell [8]. Power supply of the PhotoFET ( $v_{dd,phfet}$ ) was set to 3.3 V and the dc bias current of the PhotoFET source follower was about 40 nA, assuring a few microampere current in the PhotoFET cell and minimizing power consumption.

Later analysis showed, however, that a better noise performance could be achieved for higher source follower currents. The potential on the n-well/p-sub charge collecting diode set automatically to the level of  $v_{dd,phfet}$  decreased by the voltage

drop across the bulk-to-source junction forward biased due to the leakage current of the charge collecting diode. The potential of the virtually floating n-well implant was almost equal to the voltage of the power supply. The dc component, subtracted from the PhotoFET output current, was about 20  $\mu\text{A}$ . The main clock of 10 MHz cadenced the chip operation, defining the current sampling period at 192  $\mu\text{s}$ . There was no reset system integrated in the pixel; thus this period was equal to the signal integration time. The PB with a bonded chip was placed in a light-tight box with a constant, controlled temperature inside. Most of the tests were carried out at room temperature. The total gain of the readout chain from the pixel level to the DAS was about 200 k $\Omega$  including an internal current gain of 10.

The raw data stored to the disk were analyzed with the dedicated software, performing pedestal subtraction and noise estimation for each pixel followed by a threshold-based hit-finding analysis. In the direct current output mode, the analysis was possible individually for both samples stored in a pixel and read out separately as well as on the difference calculated with software. Particle strikes in between two readouts could be extracted, and the amount of charge released in the active detector volume could be measured.

#### B. Measurement of Fixed Pattern Noise

Fixed pattern noise (FPN), defined as a time-invariant pixel-to-pixel variation of output levels, has the same spatial arrangement and statistics from one image sample to another. Two different components fall under this noise category: dark signal nonuniformity, including deterministic shifts of signal due to mismatches of components (DSN), and charge conversion nonuniformity (CCN).

In the particle detection system, the DSN of an active pixel matrix can be much greater than the magnitude of a signal expected from a particle impact. This type of noise is relatively easy to filter out, for example, by estimating mean values for each pixel for some number of unexposed images and subtracting these means from the sample image. The construction of an intelligent particle detector aims at the system's allowing real-time extraction of particle impact events. For the compactness and efficiency of the design, all processing should be fully done on a chip. Implementation of circuit blocks, serving whole groups of pixels and taking decisions on the occurrence of an event, based on the signal height, requires equalization of the pixel output levels. Storing the whole image of mean values on the detector would require additional memory, increasing the dead area of the detector. This paper addresses elimination of DSN by subtracting samples distant in time and stored directly in each pixel. On the other hand, CCN is less detrimental in practice for a particle-tracking detector as long as it is limited to a few percent. If a high accuracy on the signal amplitude measurement is required, the appropriate correction can be applied offline on the sparsified data acquired by the DAS using a gain-mapping table.

Distributions of currents sunk by pixels in the submatrix, built with 100 fF storage capacitors, are presented in Fig. 4. This figure shows the mean values of currents for all first and second

<sup>1</sup>OPA355 amplifier, featuring input referred noise of 5.8 nV/Hz and bandwidth of 200 MHz, AD8138 differential amplifier, featuring input referred noise of 5 nV/Hz<sup>1/2</sup> and bandwidth of 320 MHz, were used for transresistance amplifiers and for unity gain buffers and differential drivers, respectively.

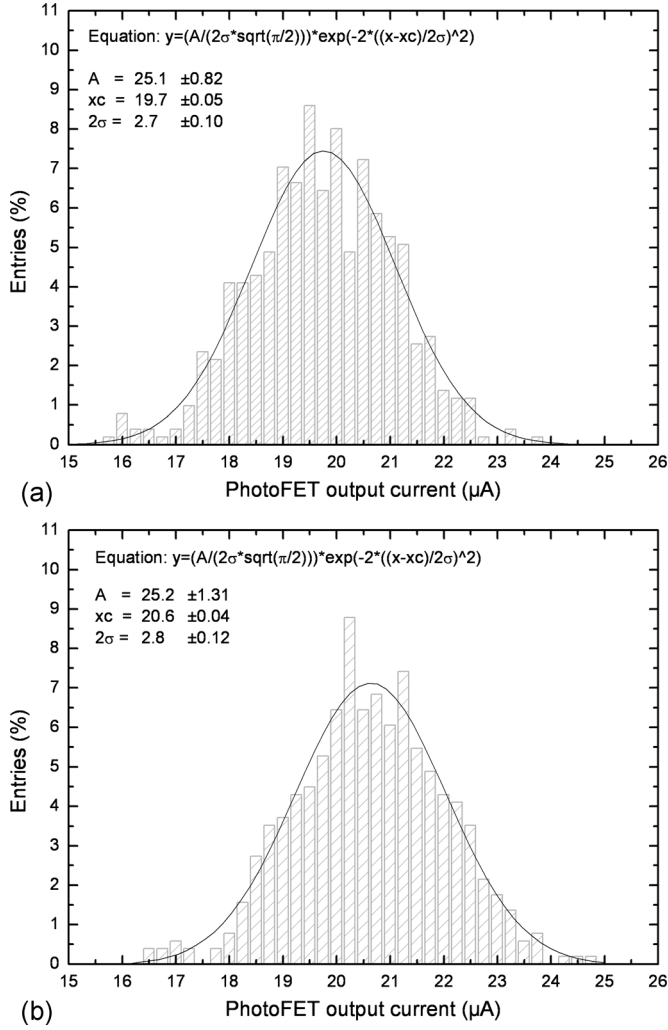


Fig. 4. Distribution of currents from PhotoFET cells of the entire matrix for (a) the first and (b) the second memory cell.

memory cells calculated for 4500 frames. The constant component, subtracted in the measurements, is included. The assumption of a Gaussian form of DSN is not always valid, especially in detectors where DSN is dominated by a spread of leakage currents of charge collecting diodes [14]. The symmetrical form of the distributions in Fig. 4 suggests that dispersion of transistor parameters, like transistor threshold voltage, geometrical dimensions, and transconductance coefficient, is the dominant effect. Gaussian fits to the distributions show the same width of about  $1.4 \mu\text{A}$  for both memory cells and mean values different by about  $1 \mu\text{A}$ . In an ideal system, current samples from both capacitors should be the same in the absence of the radiation source. A distribution of the differences between two in-pixel memory samples is shown in Fig. 5. The width of the distribution is  $65 \text{ nA}$ , indicating a factor of 20 reduction of DSN after the CDS processing. A leakage current of the charge collecting diode introduced a voltage drop across the source-bulk junction of the PMOS transistor in the PhotoFET cell. The spread of the leakage current contributed to the total current dispersions of the PhotoFET cell, shown in Fig. 4. The subtraction of the two samples, stored in the pixel, resulted in an automatic elimination of the leakage current component from DSN. However, a

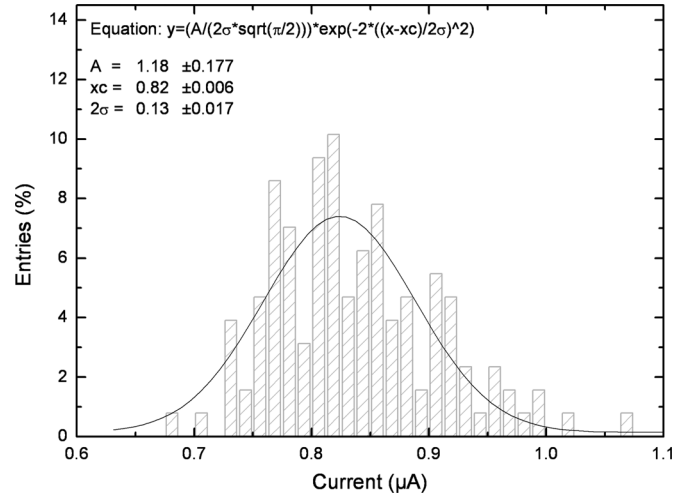


Fig. 5. Distribution of the subtraction results from the submatrix with pixels built with  $100 \text{ fF}$  storing capacitances.

significant constant shift of the mean value equal to about  $0.8 \mu\text{A}$  was still observed. The origin of the shift may be in unintended asymmetries in the layout of two memory cells or in a feedthrough between memory cells and nearby digital control lines. The effect is analyzed in the next section. This effect posed substantial problems for the operation of the current integrating transimpedance amplifiers. The shift of the mean value forced current integration with a substantial dc component that could not be subtracted as one common factor.

In classical 3T pixels, practically the only source of the signal charge-to-output conversion gain dispersion are capacitances of interconnections at the charge collecting node and spread of the junction capacitance. The dispersion does not extend past a few percent [8] in most cases. In a current mode pixel, an additional source of the dispersion is the voltage-to-current conversion. The absolute value of CCN can be expressed by

$$\Delta\text{CQI} = \text{CQV} \times g_{mt} \left( \frac{\Delta g_{mt}}{g_{mt}} + \frac{\Delta\text{CQV}}{\text{CQV}} \right) \quad (1)$$

where CQI is the charge-to-current conversion gain of the PhotoFET cell,  $g_{mt}$  is the total small signal transconductance of the PhotoFET cell, referred to the bulk-source voltage of the PMOS transistor  $M1$ , and CQV is the charge-to-voltage conversion factor proportional to the reciprocal of the charge collecting capacitance. The  $g_{mt}$  component is given by

$$g_{mt} = g_{mbM1} + g_{mM1} \times \frac{g_{mM2}}{g_{mM2} + g_{mbM2}} = g_{mM1} \times \frac{n^2 - n + 1}{n} \quad (2)$$

where  $g_{mbM1}$  and  $g_{mM1}$  are small signal transconductance parameters of the transistor  $M1$  and  $n$  is the subthreshold slope factor, assumed here to be equal for a PMOS and NMOS transistor. The drain current of a MOS transistor is a quadratic steeply raising function of its gate-source voltage. It can be concluded that the main source of current dispersions of the PhotoFET cell is pixel-to-pixel variations of the source-gate voltage of the source follower transistor  $M2$  and the threshold

voltage of the PMOS transistor  $M1$ . Assuming the operation of  $M1$  in strong inversion, the relative dispersion of the transconductance parameter is easily calculated by

$$\frac{\Delta g_{mt}}{g_{mt}} = \frac{\Delta I_{M1}}{2I_{M1}}. \quad (3)$$

Substituting numerical values, extracted from Fig. 4 to (3), the relative variation of the transconductance component is equal to about 3.5%.

During the tests, a high value of the dc compensation current for the PhotoFET cell was observed in contradiction to earlier simulations indicating only a few microamperes. The discrepancy between measurements and simulation estimations might result from an incomplete representation of the switching effects of the bias current. The bulk-to-source voltage of the transistor  $M1$  barely reaches a few tens of millivolts under constant bias conditions. Incorporation of the switching effect results in a capacitive induction of the n-well potential drop. The change of the n-well potential  $\Delta V_{n\text{-well}}$ , when bias in the pixel is switched on, is estimated by

$$\Delta V_{n\text{-well}} = \frac{C_{ox} \frac{W_{M1}}{L_{M1}} \times \Delta V_{sM2}}{C_{n\text{-well}}} + \frac{C_{bdM1} \times \Delta V_{dM1}}{C_{n\text{-well}}} \quad (4)$$

where  $C_{ox}$  is the oxide capacitance per area unit of a MOS transistor,  $W_{M1}$  and  $L_{M1}$  are geometrical dimensions of the transistor  $M1$ , and  $\Delta V_{sM2}$  and  $\Delta V_{dM1}$  are voltage steps on the source of the transistor  $M2$  and the drain of the transistor  $M1$ , respectively, at the moment of switching on the pixel.  $C_{bdM1}$  and  $C_{n\text{-well}}$  are bulk-to-source junction capacitance of the transistor  $M1$  and the total n-well region to ground capacitance, respectively. Equation (4) includes two dominant contributions only. Substituting numerical values for quantities in (4) ( $C_{ox} = 4.6 \text{ fF}/\mu\text{m}^2$ ,  $W_{M1} = 0.8 \mu\text{m}$ ,  $L_{M1} = 0.4 \mu\text{m}$ ,  $C_{n\text{-well}} = 10 \text{ fF}$  and  $C_{bdM1} = 1.5 \text{ fF}$ ), the step of the n-well potential can be estimated in the range from 300 to 500 mV. The voltages  $\Delta V_{sM2}$  and  $\Delta V_{dM1}$  were calculated, assuming that for the pixel bias switched off, the considered points drift to the power supply rail. This significant increase of the bulk-to-source voltage was identified as a source of boosting of the PhotoFET current during sampling.

### C. Measurement of Temporal Noise

An oscilloscope screenshot in Fig. 6 shows current samples converted to voltage on PB for six pixels in one column. Access times to individual pixels are marked. The first three pixels are the last pixel in one frame  $n$ , and the next three are the first pixels in the following frame  $n+1$ . The step present between two memory cells reflects the readout of two current samples of shifted values. The levels, corresponding to the cells  $Mem1$  and  $Mem2$ , are marked with (-1-) and (-2-), respectively. The distribution of 4500 signal samples for one selected typical pixel with a storing capacitance of 100 fF is presented in Fig. 7. Two histogram groups, reflecting a systematic shift between samples from both memory cells, are clearly visible. The dispersion of samples around mean values in both peaks is random and corresponds to the total temporal noise associated with the

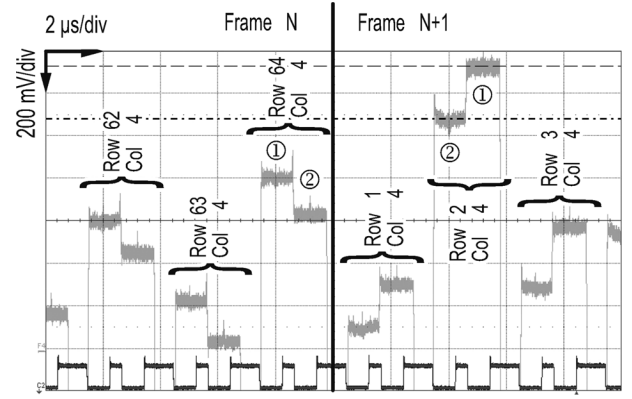


Fig. 6. Oscilloscope trace of a signal from six pixels from the same column.

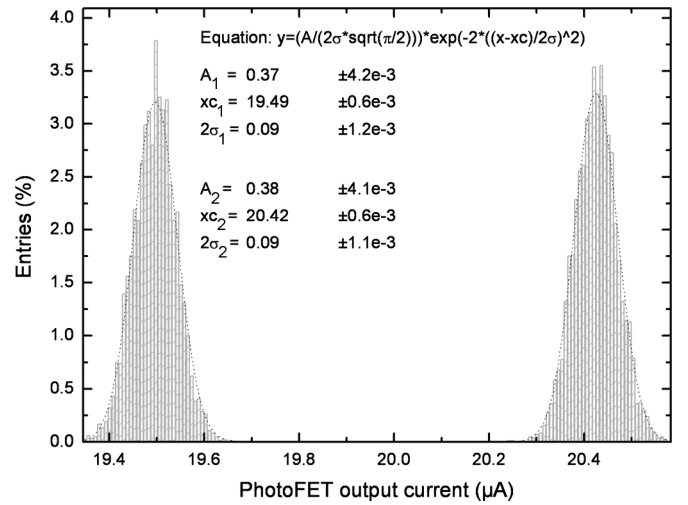


Fig. 7. Single pixel signals distribution.

pixel readout. Gaussian fits to both histogram groups yield mean values of  $19.5 \mu\text{A}$  and  $20.4 \mu\text{A}$ , respectively, with a standard deviation of 45 nA.

The systematic shift between samples can be explained as an artifact of an unequal coupling of digital signals to the plates of capacitors in two memory cells, or to the floating node of n-well in the PMOS transistor  $M1$ . In the first case, a capacitively induced voltage step results in the readout of a sample different than the stored one. In the second case, the induced voltage step on the n-well capacitance to ground is converted to current and sampled as a regular input signal. A very high sensitivity of the charge-sensing element may induce a high change of current of the transistor  $M1$ . During the design, parasitic coupling to sensitive pixel parts was minimized and equalized by symmetrical pixel layout. The control lines were separated and the capacitors were screened with a grounded *metal1* plane. The parasitic interlayer capacitances were also extracted using the DIVA tool from Cadence. The possible coupling paths to memory cells were found to be up to a few tens of attofarads. Such a capacitance is too small for their unequal distributions to induce voltage differences high enough to explain the shift observed for 100 fF memory capacitances (see Fig. 7). A postmeasurement analysis of the pixel layout revealed a 90 aF coupling capacitance between the n-well and a digital line (*metal2*), in



TABLE I  
SUMMARY OF PEDESTAL AND NOISE MEASUREMENTS

Pixel	S1-S2 (odd frame) [nA]	S1-S2 (even frame) [nA]	Standard deviation [nA] (ADCU)	DAS Noise [nA] (ADCU)
50 fF	1220	-1130	53 (21.3)	2.3 (0.9)
100 fF no comp	840	-800	38 (15)	2.3 (0.9)
100 fF comp	840	-780	38 (15)	2.3 (0.9)

a 0.4  $\mu\text{m}$  distance, activating a charge injection compensation switch. The change in the output current is equal to about 1.1  $\mu\text{A}$  for the digital signal transition from 3.3 to 0 V, with a 10 fF n-well ground capacitance and the total transconductance of the charge sensing element  $g_{mt}$ , equal to about 45  $\mu\text{S}$ . It shows a close agreement with the shift observed in Fig. 7. The coupling can be avoided by introducing shielding around the n-well region and increasing spacing to all control lines on a next prototype. The shift is systematic with a small variation around the mean value. Subtracting different programmed current values for even and odd frames can eliminate it.

The statistical analysis on differences of two current samples from in-pixel memory cells was carried out for each submatrix. The noise performance of the system was measured. The measurements were done at the temperature range from 0 to 30  $^{\circ}\text{C}$  and frequencies of the main clock from 10 to 50 MHz, translating to the frame integration time from 19.2 to 3.8 ms. Pedestals and noise were independent on temperature and clock frequency within the ranges examined. The same variance was measured for current samples from both memory cells. The results, including the mean value for odd and even frames and temporal noise for the whole system with and without the MVII chip, are shown in Table I. The noise level is significantly higher for the pixel with a smaller memory cell capacitance. No difference was observed between the pixel design featuring dummy switches to compensate for charge injections and the design where the compensation switches were not connected. This measurement shows that the additional circuit complexity is not justified. An example distribution of 4500 current samples, after the CDS operation (done in software), is presented in Fig. 8 for a single, arbitrarily chosen pixel with 100 fF storing capacitance. To simplify these studies, only one pedestal polarity was delivered by separately analyzing odd and even frames.

The tests of direct current outputs required using internal current mirrors with a gain of 10 and a bias current in the input branch of a current mirror of 50  $\mu\text{A}$ . In this configuration, the optimum noise performance was not reached; however, the noise contribution from the external stage was negligible. The bandwidth of the PhotoFET circuit during sampling  $f_{\text{up1}}$  was defined by

$$f_{\text{up1}} = \frac{g_{mMm1,Mm4}|_s}{2\pi C_{gMm1,Mm4}} \quad (5)$$

where  $g_{mMm1,Mm4}|_s$  is a small signal transconductance of current sampling transistors in a pixel in active state during sampling and  $C_{gMm1,Mm4}$  is the capacitance of a memory cell.

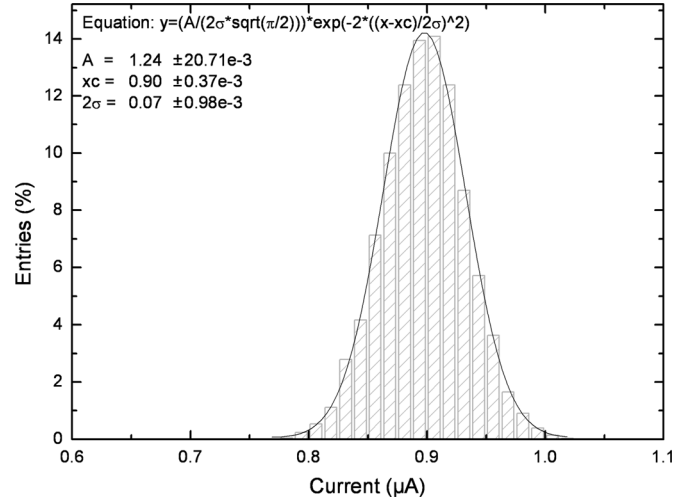


Fig. 8. Distribution of a single pixel current output after CDS operation ( $C = 100$  fF) for one frame direction.

The capacitance  $C_{gMm1,Mm4}$  is not constant between sampling and readout periods. The transistors  $Mc1$  and  $Mc2$ , used for extracting average current in a row, are turned off during sampling of the current from transistor  $M1$  and turned on during the readout. This decreases the capacitance  $C_{gMm1,Mm4}$  during the readout phase by a factor of about 1/3 of the gate oxide capacitance of  $Mc1$  and  $Mc2$  and results in an increase of the memory current by a certain factor  $G$ . The system's bandwidth is limited by the transresistance amplifiers placed on PB. It was estimated, in simulations with proprietary SPICE models of operational amplifiers, to be about  $f_{\text{up2}} = 20$  MHz during the readout phase. The bias and bandwidth of the pixel in the current design were not optimized for the best noise performance. The selection of current and bias voltages was done bearing flexible testing and study of performances in different conditions. The bandwidth of the PhotoFET, not limited by any additional capacitive load, led to sampling of noise on the current memory cells in a bandwidth much wider than required by the read out speed. The bandwidth of the PhotoFET cell  $f_{\text{up1}}$  was equal to about 200 MHz and about 70 MHz for  $C_{gMm1,Mm4}$  equal to 50 and 100 fF, respectively, at the readout current of the PhotoFET cell of about 20  $\mu\text{A}$ . Identification of main noise contributors and correlation of noise calculation with noise measurements, presented further in this section, can be used as guidelines for next designs. The transistors, contributing in a significant amount to the total output noise, can easily be targeted and their contributions quantified. The root mean square current noise values referred to the output node  $I_{pix}$  from pixel are given by (6)–(10), shown at the bottom of the next page, where  $k$  is Boltzmann's constant,  $T = 300$  K, and all  $g_m$  components represent small signal transconductances. The subscript indexes at symbols of individual current noise components refer to appropriate transistors. The last equation represents noise of the current buffer with two sums of transistor transconductances at the input and the output of the current mirror, including the transistors used for the subtraction of the dc current component. Substituting numerical values, estimated at the chosen operating point used in noise measurements ( $g_{mM2} = 20.0$   $\mu\text{S}$ ,  $g_{mM1} = 44.0$   $\mu\text{S}$ ,  $g_{mbM1} = 6.9$   $\mu\text{S}$ ,  $g_{mMsf1} = 10.9$   $\mu\text{S}$ ,  $g_{mMm1,Mm4}|_s =$

$44.0 \mu\text{S}$  ( $63.0 \mu\text{S}$ ),  $g_{mMm2,Mm5}|_r = 49.0 \mu\text{S}$  ( $69.3 \mu\text{S}$ ),  $G = 1.2$ ), the constituent noise contributions are equal to  $\langle i_{M2} \rangle = 11.0 \text{ nA}$  ( $18.3 \text{ nA}$ ),  $\langle i_{Ms f1} \rangle = 8.1 \text{ nA}$  ( $13.5 \text{ nA}$ ),  $\langle i_{M1} \rangle = 8 \text{ nA}$  ( $10.5 \text{ nA}$ ),  $\langle i_{Mm1,Mm4} \rangle = 8.5 \text{ nA}$  ( $15.3 \text{ nA}$ ), and  $\langle i_{\sum M I gain} \rangle = 12 \text{ nA}$ . The first values were calculated for  $100 \text{ fF}$  capacitances and the values in brackets for  $50 \text{ fF}$  capacitances. The total noise current  $\langle i_{total} \rangle = 22 \text{ nA}$  ( $32 \text{ nA}$ ). For the subtraction of two samples, the final theoretical noise value increases in approximation by a factor  $\sqrt{2}$  resulting in  $\langle i_{totalCDS} \rangle = 31 \text{ nA}$  ( $45 \text{ nA}$ ). The presented noise analysis includes only thermal noise. Flicker noise was not considered, assuming its partial reduction in the subtraction process. The use of the current buffer was only provisional in MVII. The goal was to use a low-noise integrated transresistance amplifier. Substitutions of numerical values in (6)–(10) reveal that the dominant noise contribution comes from the source follower. The methodology to decrease this noise is to limit the bandwidth of the PhotoFET pixel during current sampling and to increase the transconductance of the transistor  $M2$ . The bandwidth of the PhotoFET cell in MVII was incommensurably wide with respect to the pixel's switch-on time. The bandwidth could be reduced as far as it would allow correct settling of signals when the pixel is powered on. The rate at which an individual pixel can be addressed is determined by the transfer of signals from a pixel to the column end. Usually, column lines are loaded with multicofarad capacitances. Hence, a frequency of the clock selecting pixels may be up to a few tens of megahertz. Having as much time for in-pixel current sampling as for reading out the sampled data from pixel, the bandwidth of the PhotoFET cell can be decreased in the optimized design by several times with respect to the current design. The result will be a similar degree of noise reduction. The transconductance of  $M2$  can be increased by allowing more current in the source follower. The absolute noise contribution of the source follower increases with increasing transconductance of the transistor  $M1$ . However, the noise, referred to the n-well node, depends

only on the transconductances of  $M2$  and the diode-connected transistors  $Mm1$  and  $Mm2$  in memory cells. The increase of the gate-to-source voltage of the source follower transistor translates to an increase of the current in  $M1$  and memory cell transistors. Their transconductances and noise spectral densities of noise sources associated with these transistors increase accordingly. The transconductances increase proportionally, making the input referred ENC independent of the current in the branch  $M1 - Mm1$  ( $-Mm2$ ). The noise contribution of transistors  $Mm1$  and  $Mm2$  is proportional to the square of their transconductances; thus these transistors, as well as the transistor  $Ms f1$ , should be designed with the minimized width-to-length ratio. It was observed in the measurements that, at the constant source follower bias current, the current in the transistor  $M1$  increased with the increasing power supply  $vdd\_phfet$ . The effect resulted from a strong body effect showed by the transistor  $M2$ . The increase of its gate potential and higher gate-to-source voltage both lead to the increase of current of the transistor  $M1$ . The increased current and transconductance of  $M1$  has no effect on noise originating in the PhotoFET cell but allows reducing noise contributions to the input referred ENC from signal processing stages placed downstream. The illustration of the simulated input-referred ENC is shown in Fig. 9 as a function of the PhotoFET bias conditions for the current design. The optimal operating point lays at the source follower currents above  $1 \mu\text{A}$ . A reasonable value for the bias current of the transistor  $M1$ , regarding power consumption and dynamic swing, was found equal to about  $15 \mu\text{A}$  for  $vdd\_phfet$  equal to  $2.7 \text{ V}$ . The simulation results obtained with SPECTRE from Cadence after the first measurements suggested operation at higher bias currents than initially considered.

#### D. Measurement of Detector Conversion Gain

The aim of the calibration was to estimate the charge-to-current conversion factor and in the consequence ENC for the

$$\langle i_{M2} \rangle = \sqrt{\int_0^{f_{up1}} \frac{8}{3} kT \frac{1}{g_{mM2}} g_{mM1}^2 G^2 df} \quad (6)$$

$$\langle i_{Ms f1} \rangle = \sqrt{\int_0^{f_{up1}} \frac{8}{3} kT \frac{g_{mMs f1}}{g_{mM2}^2} g_{mM1}^2 G^2 df} \quad (7)$$

$$\langle i_{M1} \rangle = \sqrt{\int_0^{f_{up1}} \frac{8}{3} kT g_{mM1} G^2 df + \int_0^{f_{up1}} \frac{8}{3} kT g_{mbM1} G^2 df} \quad (8)$$

$$\langle i_{Mm1,Mm4} \rangle = \sqrt{\int_0^{f_{up1}} \frac{8}{3} kT g_{mMm1,Mm4}|_s G^2 df + \int_0^{f_{up2}} \frac{8}{3} kT g_{mMm1,Mm4}|_r df} \quad (9)$$

$$\langle i_{\sum M I gain} \rangle = \sqrt{\int_0^{f_{up2}} \frac{8}{3} kT \left( \sum_{input} g_{mNMOS,PMOS} \right) df + \int_0^{f_{up2}} \frac{8}{3} kT \frac{1}{10} \left( \sum_{output} g_{mNMOS,PMOS} \right) df} \quad (10)$$

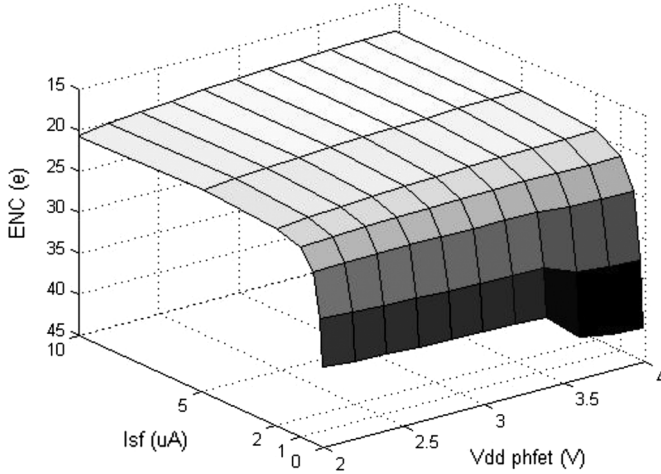


Fig. 9. Simulation of ENC versus bias current of the source follower and power supply voltage for the implementation of the PhotoFET cell in MVII.

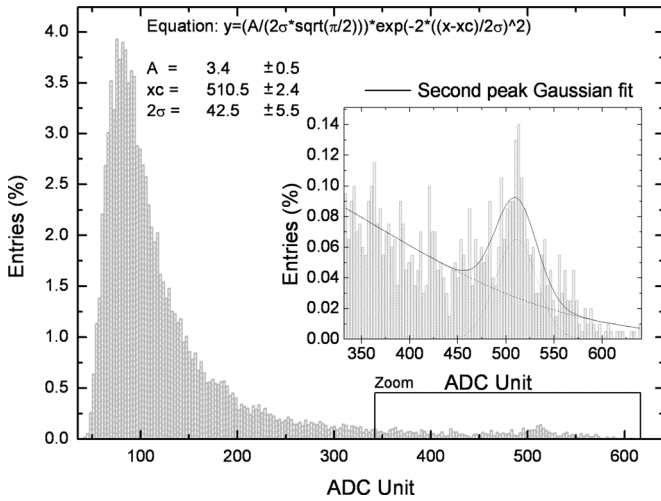


Fig. 10. Distribution of signals from single pixels for SNR above five.

PhotoFET cell in a matrix structure. The calibration was carried out using a standard spectroscopy with 5.9 keV X-rays from a  $^{55}\text{Fe}$  source [5]. The distribution of signals from single pixels in MVII is shown in Fig. 10. The spectrum was obtained from one million frames and application of a signal-to-noise ratio (SNR) cut above five. The two peaks visible in the spectrum correspond to the thermally diffused charge that is collected by a single pixel (mean value about 100 ADCU) and the complete collection of the  $1640\text{ e}^-$  liberated by an X-ray photon (about 510 ADCU). One ADCU corresponded to  $500\text{ }\mu\text{V}$  and the transimpedance gain of the analog chain was  $200\text{ k}\Omega$ . The charge-to-current conversion factor was estimated to about  $770\text{ pA/e}^-$ . The absolute value of ENC at the optimal bias current configuration was about  $50\text{ e}^-$  after the CDS processing.

#### IV. IMPLEMENTATION OF CDS

##### A. CDS Using Discrete Components

1) *Design of Processing Circuitry:* The on-flight extraction of signals from particles, impinging the MVII sensor, requires

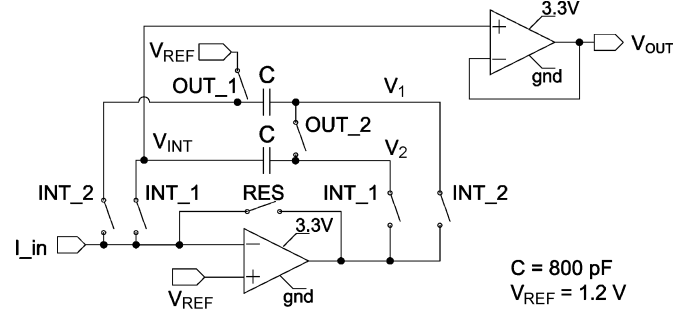


Fig. 11. Schematic diagrams of the circuit realizing CDS operation.

a low offset circuitry subtracting two current samples delivered by each pixel at column ends on the chip. The architecture proposed was a circuit integrating two current samples and subtracting resulting voltages. It was optimized for high gain, operation speed, good noise performance, minimized power consumption, and least area occupied. The subtraction through the capacitor arithmetic principle requires using nonideal switches that may introduce and excess noise [15]. On the other hand, a part of low-frequency noise of the amplifier, sampled on two memories, could be subtracted together with signals. The estimation of pixel-to-pixel dispersions of currents had a considerable bearing on the functionality of the circuit. The design kit for the process used did not contain enough information to assess these dispersions during the design. In order to validate the readout approach with current integrating transimpedance amplifiers and DAS developed, a topologically identical block was realized using discrete components. It employed one operational amplifier and two integrating capacitors switched successively in the feedback path.

In a discrete realization, all parasitic capacitances are three orders of magnitude bigger than in the integrated counterpart. Large integrating capacitors, longer integration time, and additional signal amplification were implemented to compensate for charge sharing on parasitic capacitances and to measure voltage signals comparable to the integrated version. Discrete transistor switches (ADG712) with the input and output capacitances of a few picofarads,  $800\text{ pF}$  current integrating capacitor, and current conveyor with a gain of 100 were used. Optimum performance was achieved with fast, low noise CMOS operational amplifier OPA355. The schematic diagram is shown in Fig. 11.

The operation of the transimpedance amplifier requires two integration phases. Each phase, controlled with  $INT\_1$  and  $INT\_2$  signals, begins by asserting the  $RES$  signal for resetting the associated current integrating capacitor. During the integration phase, the current sample is converted into voltage on the feedback capacitor according to

$$V_{cap1,2} = \frac{I_{1,2} \times T_{1,2}}{C_{1,2}} \quad (11)$$

where  $T$  is the integration time and symbols 1, 2 distinguish between the first and second sample. The output signal is read out by connecting both capacitances in series with  $OUT\_1$  and

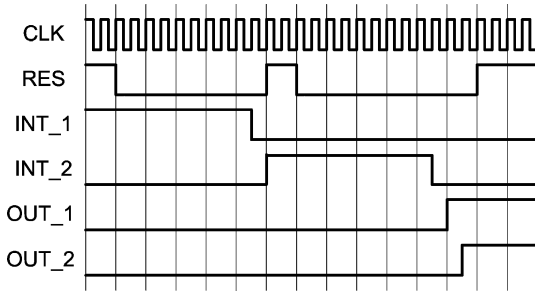


Fig. 12. Timing diagram of digital signals for driving the CDS block.

$OUT_2$  signals and clamping one of terminals to a stable reference potential. The resulting voltage equals the reference level shifted by the difference of two samples

$$\begin{aligned} V_{OUT} &= V_{REF} + V_{cap1} - V_{cap2} \\ &= V_{REF} + \frac{I_1 \times T_1}{C_1} - \frac{I_2 \times T_2}{C_2} \\ &= V_{REF} + \Delta I \times \frac{T}{C} \end{aligned} \quad (12)$$

where  $V_{OUT}$  is the output voltage during the readout phase,  $V_{cap1,2}$  are signal voltages sampled on both integrating capacitances, and, assuming  $C_1 = C_2 = C$  and  $T_1 = T_2 = T$ , the theoretical gain is equal to  $T/C$ . Introducing  $T = 0.9 \mu s$  and  $C = 800 pF$  and the entrance current gain of 100, the transimpedance gain equals 112 k $\Omega$ .

The timing diagram for controlling signals is presented in Fig. 12. All signals were synchronous to the operation of the MVII chip. The maximum frequency of the main clock for the integrated solution was assessed in ELDO transient simulations to be 10 MHz. The total transimpedance gain of the readout chain from the pixel level to DAS was estimated at about 180 k $\Omega$ .

The expected low-noise performance was confirmed with transient noise simulations, as appropriate for switched capacitor circuits, performed with the ELDO simulator.<sup>2</sup> Low root mean square (rms) noise voltage at the output of the circuit results from a partial correlation of noise generated by the operational amplifier in the samples stored on both integrating capacitances. The correlated component of noise is removed during the readout phase as a result of the capacitance arithmetic

$$\begin{aligned} V_{OUT} &= V_{REF} + (V_{cap1} + V_{nc1} + V_{nn1}) \\ &\quad - (V_{cap2} + V_{nc2} + V_{nn2}) \\ &= V_{REF} + (V_{cap1} + V_{nc1}) - (V_{cap2} + V_{nc2}) \end{aligned} \quad (13)$$

where  $V_{nc1,2}$  is the correlated component of the sampled noise and  $V_{nn1,2}$  are not correlated noise components, sampled on the first and the second integrating capacitance. The transimpedance amplifier tracks the same noise performance tendency in the range of the simulated integration times from 0.22 to 5.5  $\mu s$ .

<sup>2</sup>MentorGraphics.

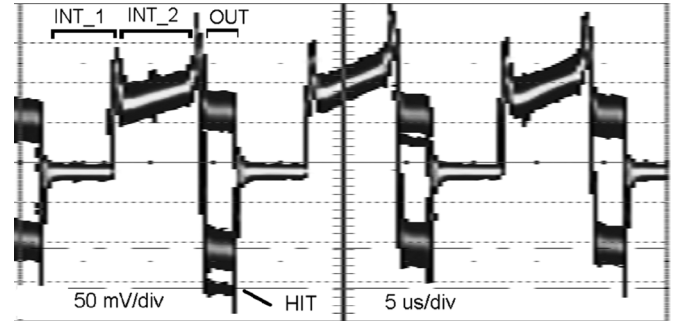


Fig. 13. Oscilloscope output signal waveforms observed at one line of the differential output of the proximity board.

2) *Tests With Direct Current Outputs of MVII:* The discrete transimpedance amplifier was tested with direct current outputs of the MVII chip. The bias conditions of the PhotoFET cell were set to  $v_{dd\_phFET} = V_{dd\_sf} = 3.0 V$ ,  $I_{sf} < 100 nA$ . The average value of current, sourced by a PhotoFET cell, was 15  $\mu A$  for these conditions. The bank of the on-chip current amplifiers was used to provide a current gain of 10 for the output signals. An additional current gain of ten was implemented on PB.

The results of noise measurements of the chip with the readout chain indicated noise of 65 nA (22.0 ADC), 50 nA (17.0 ADC), and 48 nA (16.5 ADC) for pixels with 50 fF memory capacitors, 100 fF capacitors without switches compensating for charge injection, and 100 fF capacitor with the compensating switches, respectively. All measurements were carried out for the chip under tests kept in a light-tight box and at ambient but not stabilized temperature. It is noticeable that the first 16 pixels featuring the smallest, 50 fF memory capacitance, exhibit the highest noise. The dominant source of noise is in a pixel. There was only a small contribution to the total noise from a part of the readout chain, remaining after disconnecting the MVII chip. The sensor was also exposed to X-ray photons from a  $^{55}Fe$  source. An example of the voltage waveforms recorded with an oscilloscope is presented in Fig. 13. Time intervals, marked in Fig. 13 as  $INT_1$ ,  $INT_2$ , and  $OUT$ , correspond to the first and second integration (0.9  $\mu s$ ) and the readout phase (0.4  $\mu s$ ), respectively. The waveform is shown using the *persistence* operation mode of the oscilloscope. There are two voltage levels in the readout phase that correspond to even and odd frames. Random events, with large difference in the output voltage level, marked as *HIT*, correspond to the prints of X-ray photons. A histogram of data from even frames is shown in Fig. 14. The histogram was built for the SNR cut equal to ten. A very similar histogram was built for odd frames. The amplitude of the calibration peak can easily be extracted at about 470 ADCU. The peak position translates to CQI of the PhotoFET cell equal to about 840 pA/e $^-$ .

The width of the calibration peak carries information about pixel-to-pixel dispersions of the conversion gain. The Gaussian fit to the calibration peak yields  $\sigma_p = 23.6 ADCU$ . The width of the peak is a quadratic sum of temporal noise  $\sigma_t$ , dispersion of the conversion gain due to the differences of the bias current of the transistor  $M1$  between pixels,  $\Delta CQI_I$ , and the spread of the conversion gain due to pixel-to-pixel variation of the n-well/p-sub capacitance  $\Delta CQI_C$ . The dispersion of the charge

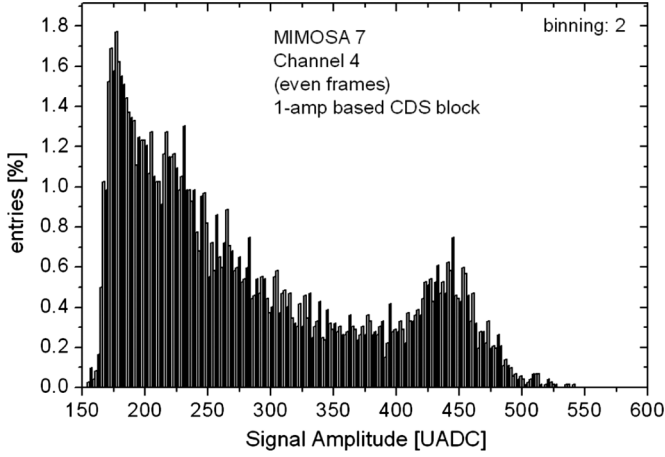


Fig. 14. Spectrum of X-ray photons obtained for pixels with 100 fF memory capacitors. The Gaussian fit to the calibration peak gives  $\sigma_p = 23.6$  ADCU.

to current conversion factor due to the spread of n-well/p-sub capacitances is given by

$$\Delta CQI_C = \sqrt{(\sigma_p)^2 - ((\Delta CQI_I)^2 + (\sigma_t)^2)} \quad (14)$$

$\sigma_p$  is calculated from the width of the calibration peak and  $\sigma_t$  is the temporal noise measured. Substituting a numerical value for  $\Delta CQI_I = 3.5\%$ , as was estimated in one of the previous chapters,  $\Delta CQI_C$  equals to about 2.9%. It is a typical value for classical photodiode active pixel sensors.

### B. Integrated CDS

1) *Architecture of the Readout Chain:* A conceptual schematic of the MVII transimpedance amplifier, placed at the ends of eight pixel columns, is shown in Fig. 15. A careful approach to the design of a physical layout of the circuitry was critical for minimizing all parasitic effects. Characteristic to the integrated implementation is the association of each switch transistor with its counterpart to compensate for charge injection from a transistor channel and to eliminate feedthrough of control signals. No charge injection compensation switches are depicted in Fig. 15 for the sake of clarity. An additional switch, connecting the *column* input line to the reference voltage of 1.2 V and activated by the *PCH* signal, allows precharging a parasitic stray capacitance of the column line before each integration phase. The integrating capacitances, implemented in the design, are 200 fF each. The operational amplifier design is a classical two-stage folded cascode amplifier with the dc gain of 72 dB and the unity gain frequency of 66 MHz. The ideal transimpedance gain equals to 500 k $\Omega$  according to (12) for the integration time of 100 ns. The gain in the postlayout simulations was reduced almost by half to 280 k $\Omega$ . The decrease resulted from attenuation of signal on a capacitive divider between the equivalent capacitance of a series connection of two current integrating capacitances and the parasitic input capacitance of the voltage buffer. The expected noise level during the readout phase, estimated in transient noise simulations with ELDO, was about 300  $\mu$ V rms. This corresponds to about 1 nA rms of the input referred noise. The estimated ENC would

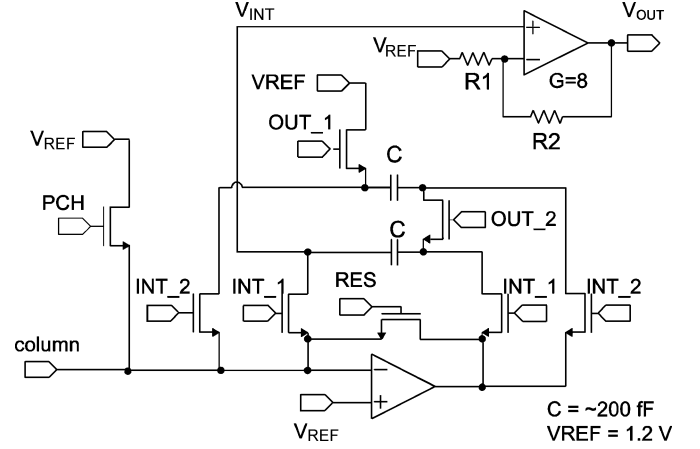


Fig. 15. Schematic diagram of the MVII current integrating transimpedance amplifier.

be less than two electrons for the charge-to-current conversion factor of 770 pA/e $^-$ .

2) *Feedback From Tests:* A large pixel-to-pixel dispersion of currents, almost 9  $\mu$ A peak-to-peak (Fig. 4), was measured in the tests of direct current outputs. Together with the additional difference in the value of samples between two memory cells in one pixel of about 1  $\mu$ A, this led to the saturation of the CDS circuit. The high amplifier gain allowed maximum input dc current to be only about 2  $\mu$ A impeding full functionality tests. Dispersion of currents was underestimated in the design due to the lack of the measurement data from PhotoFET cell and the inadequate simulation model.

In addition, an external access to the amplifiers had not been foreseen, limiting the possibilities of testing the chip to conversion of a constant current from the dc component compensation circuit while the pixel readout was disabled by the appropriate control pattern loaded to the chip. A fast switching between two values of external current was impossible due to low bandwidth of this path. Instead, different integration times for two samples were used. The gain was estimated varying integration times from 60 to 100 ns. The transimpedance amplifier was connected to a differential buffer in a non-inverting configuration with a gain of eight, as shown in Fig. 15. The output voltage, using the basic ideal operational amplifier theory, is calculated in this configuration by

$$V_{OUT} = V_{INT} \left( 1 + \frac{R_2}{R_1} \right) - V_{REF} \frac{R_2}{R_1}. \quad (15)$$

In the notation for the ideal operation of the circuit, the voltage at the output of the transimpedance amplifier is given by

$$V_{INT} = V_{REF} + I \times \frac{\Delta T}{C} \quad (16)$$

where  $I$  is a constant value of the integrated current and  $\Delta T$  is a difference between both integration intervals. Substituting (16) into (15) and subtracting the reference voltage from the  $V_{OUT}$ ,

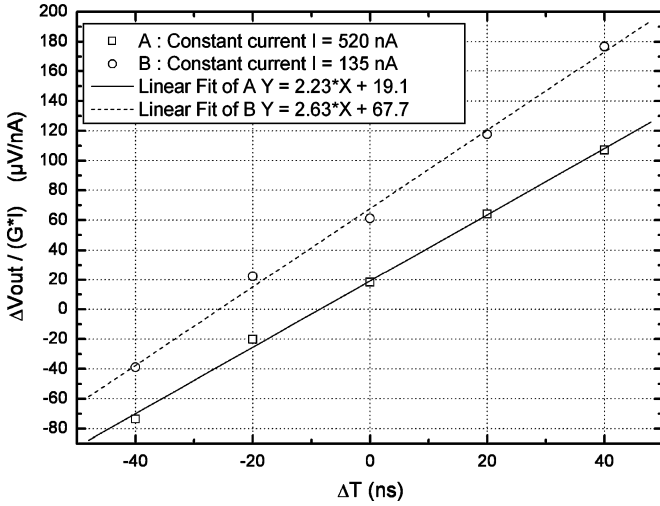


Fig. 16. Gain of the MVII transimpedance amplifier for two values of the integrated current used as a parameter.

the estimation of the effective integration capacitance can be derived

$$\frac{\Delta V_{OUT}}{\left(1 + \frac{R_2}{R_1}\right) \times I} = \frac{\Delta T}{C}. \quad (17)$$

Fig. 16 illustrates this formula for two different values of the input current, i.e., 135 and 520 nA. The inverse of the slope of the linear fit to the measurement point gives directly the equivalent value of the integration capacitors. The transresistance gain of the amplifier can be calculated assuming the default integration time equal to 100 ns. The two fits yield slightly different capacitance values, i.e., 380 and 448 fF for input current equal to 135 and 520 nA, respectively. The gain is accordingly equal to 263 and 223 k $\Omega$  and is in agreement with the simulation results. The offset between the two fits in Fig. 16 at  $\Delta T = 0$ , and different slopes reveal dependency of the circuit response on common and differential components of the integrated currents. The equivalent values of current integrating capacitances change due to a nonlinear, signal-dependent charge sharing between capacitances in the feedback path and the parasitic capacitances, for example, junction capacitances of the transistor switches. The performance of the integrated transimpedance amplifier can be improved by implementing larger current integrating capacitances. The drop in the transresistance gain could be compensated by an additional current amplifying stage placed upstream.

## V. CONCLUSIONS

The M7 prototype was the first embodiment of the PhotoFET cell in a full matrix of pixels, including analog and digital readout circuitry implemented on the same chip. The readout of the chip was organized in a column parallel way for the readout speed. The cell was characterized by a high, almost 1 nA/e<sup>-</sup> conversion factor (found in calibration with a <sup>55</sup>Fe source) and featured two current mode memory cells for the CDS operation, aiming at future implementation of the full

sparsification processing to create an autonomous, intelligent charged particle detector. The increased noise (ENC = 50 e<sup>-</sup>), found in the measurements with the MVII chip was unexpected. However, the noise analysis allowed identifying the source of noise and drawing guidelines for the next optimized prototypes. The noise performance can be improved by lowering the bandwidth of each part of the analog chain according to the goal requirements. The bandwidth of the PhotoFET cell can be decreased in the optimized design by several times with respect to the current design, resulting in a corresponding degree of noise reduction. The pixel design requires bigger in-pixel sampling capacitances, improving also the immunity of the design to any external interference. Also other problems, found in the measurements, like a constant shift between two current samples from two memory cells in each pixel or an increased value of the PhotoFET bias current were understood and quantified paving the way for future improvements. The modular test bench, developed for flexible and efficient testing of different MAPS prototypes, was presented. Unfortunately, this combination of a pixel and the integrated current signal treatment was not possible to be tested as one entity, due to the bigger than expected current dispersion of the PhotoFET. However, all ideas presented and building blocks tested were verified to be functional.

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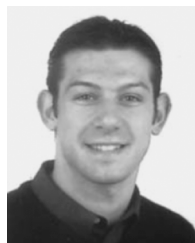
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